REMARKS

The comments of the Applicant below are each preceded by related comments of the Examiner (in small, bold type).

Claims 13, 49, 55, 56 and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by Correale, Jr. et al. [US 6,587,905 B1] (hereinafter "Correale").

Per claims 13, 49, 55, 56 and 61, Correale teaches a data processor (see Correale, claim 4, "a data processing system", the processor is considered to be including the CPU, other Master devices, and the PLB Arbiter) comprising:

a plurality of programming engines (see Fig. 10, the Master devices);

a push arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of an unidirectional push bus (see Fig. 10, rdDBus) by a plurality of external memory resources that are external to the data processor (see Fig. 10, the Slave devices), the push bus arbiter being internal to the data processor (see col. 4, lines 1-6, PLB and its arbiter are comprised within the processor architecture), the push bus to push data from the memory resources to an input transfer memory (not clearly shown by Correale in its drawings, but it is clear that a register must be present on a processor's input port which is connected to a data bus in a processor architecture, because processors can execute instructions and fetch data much faster than memories can be accessed to provide the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a system clock) associated with the programming engines; and

a pull bus arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of a unidirectional pull bus (see Fig. 10, wrDBus) by the external memory resources, the pull bus arbiter being internal to the data processor, the pull bus to pull data from an output transfer memory (not clearly shown by Correale, but it is clear that a register must be present on a processor's output port which is connected to a data bus in a processor architecture, because processors can execute instructions and provide read/write data much faster than memories can be accessed to provide or store the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a clock) associated with the programming engines and to transfer the data to the memory resources.

Correale does not describe and would not have made obvious "a plurality of memory resources, each memory resource being associated with a memory controller," "a push bus arbiter to arbitrate use of the push bus by the memory resources in which requests for using the push bus are sent from the memory resources," and "a pull bus arbiter to arbitrate use of the pull bus by the memory resources in which requests for using the pull bus are sent from the memory resources," as recited in amended claim 13.

Correale discloses an arbiter that grants bus access to requesting master devices (col. 2, lines 29-30, col. 7, lines 14-15, col. 8, lines 21-22). Correale does not disclose or suggest an arbiter that arbitrates requests from the slave devices. If the Examiner contends that the "slave devices" in Correale correspond to the "memory resources" of claim 13, Correale does not

disclose or suggest arbitrating use of the data buses by the memory resources in which requests for using the buses are sent from the memory resources, as recited in claim 13.

Claims 26, 49, 55, 56 and 61 are patentable for at least similar reasons as those applied to claim 13.

> **Claims 1-7, 16-21, 26-29, 33-35, 37, 40, 41, 43-45. 50, 51, 53, 54 and 57-60 are rejected under U.S.C. 103(a) as being unpatentable over Correale and Shaylor [US 6,408,325 B] (hereinafter "Shaylor").**
>
> **Per claims 1, 26 and 37, it is clear the Correale already teaches most of the claims as described above (the programming agent in claim 56 is considered to be equivalent to the processing agent of claim 1), and further teaches issuing a write command (the pulling of data from the processing agent to the memory resources must be a result of a write command) and loading data into an output transfer memory of the processing agent (see the rejection of claims 13, 49, 55, 56 and 61 above). Correale also discloses setting the output transfer memory to a read-only state, even though it does not explicitly recite this limitation. However, it should be clear that since processors can execute instructions and issue memory write request much faster than the actual write operations can be completed by accessing the much slower memory, the processor's output register must have its write enable control signal disabled while the data to be written to memory is ready to be transferred over the data bus, in order to avoid the data being overwritten by a new write data generated by the processor before the current transfer is complete.**
>
> **Correale does not teach executing a context. Shaylor teaches a multi-tasking and multi-threading processor that can enhance data processing efficiency (see Shaylor, col. 1, lines 46-50), the processor requires executing a context for each thread (see Shaylor, col. 1, lines 56-67). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine the teachings of Shaylor and Correale, in order to enhance data processing efficiency. As a result of the combination, Correale and Shaylor in combination teach "executing a context".**

Correale does not describe and would not have made obvious "using a push bus arbiter to arbitrate use of a push bus by the memory resources in which requests for using the push bus are sent from the memory resources," and "using a pull bus arbiter to arbitrate use of a pull bus by the memory resources in which requests for using the pull bus are sent from the memory resources," as recited in amended claim 1.

Correale discloses an arbiter that grants bus access to requesting master devices (col. 2, lines 29-30, col. 7, lines 14-15, col. 8, lines 21-22). Correale does not disclose or suggest an arbiter that arbitrates requests from the slave devices. Even if the Examiner contends that the "slave devices" in Correale correspond to the "memory resources" of claim 13, Correale does not disclose or suggest arbitrating use of the data buses by the memory resources in which requests for using the buses are sent from the memory resources, as recited in claim 1.

Claim 37 is patentable for at least similar reasons as those applied to claim 1.

Regarding new claim 62, Correale does not describe and would not have made obvious a push bus arbiter to arbitrate use of the push bus by the memory resources and a pull bus arbiter to arbitrate use of the pull bus by the memory resources, wherein the memory resources comprise random access memory devices, as recited in claim 62. Rather, Correale discloses slave devices that can be, e.g., a memory controller or a PCI bridge (col. 5, lines 57-58). Even if a PCI bridge includes buffers that store data, the buffers of a PCI bridge is different from a random access memory device.

Regarding new claim 63, Correale does not describe and would not have made obvious each of the requests for use of the push bus or pull bus from the memory resources comprises a target identifier identifying a target to receive data pushed from or pulled to the memory resources. Correale discloses an arbiter that grants bus access to requesting master devices (col. 2, lines 29-30, col. 7, lines 14-15, col. 8, lines 21-22). Correale does not disclose or suggest that requests for use of the push bus or pull bus are sent from the memory resources, let alone requests that each comprises a target identifier identifying a target to receive data pushed from or pulled to the memory resources.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Any circumstance in which the applicant has addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner. Any circumstance in which the applicant has made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims. Any circumstance in which the applicant has amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply the Excess Claims fee (if any) and any other charges or credits to deposit account 06-1050, referencing attorney docket no. 10559-618001.

Respectfully submitted,

Date: March 17, 2008

/Rex I. Huang/
Attorney for Intel Corporation
Rex I. Huang
Reg. No. 57,661

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

21878032.doc